CENG3430 2020-21 Online Final Exam

- The final exam of CENG3430 will be conducted ONLINE from 9:30am to 11:30am on May 3, 2021.
 - It's an **OPEN BOOK** and **PAPER-FORM** exam.
 - Its scope covers Lec01~Lec10 and Lab01~Lab10.
 - It will be organized into the following three phases:
 - ① ID Verification (9:30am to 9:50am)
 - ✓ Join this Zoom session using your computer with webcam;
 - ✓ Show your face and student ID card (or ID card) to our tutors;
 - ② Answering (9:50am to 11:30am)
 - ✓ Download the <u>final exam papers</u> from Blackboard;
 - ✓ Write down answers on <u>blank A4 papers</u> (prepared by yourself);
 - **③** Submission (after 11:30am, NO early-submission)
 - ✓ <u>Take clear photos</u> of what you have written on A4 papers;
 - \checkmark Submit all the photos to Blackboard.

- Contact us if you have any problems/difficulties ASAP.

① ID Verification (9:30am to 9:50am)



- 1) Join this <u>Zoom session</u> with your CUHK account (student-ID@link.cuhk.edu.hk) using your computer with webcam.
 - The passcode is **#CENG3430**.
 - Stay "Muted" and "Start Video" on Zoom as follows:



- If your computer is not equipped with a webcam, you can use your cellphone to join the Zoom session instead.
- 2) Show your <u>face</u> and <u>student ID card</u> (or <u>ID card</u>) to our tutors through the webcam (or your cellphone).

② Answering (9:50am to 11:30am)



- 1) Download the **final exam papers** (in **PDF** format) from **Blackboard** (after 9:50am on May 3, 2021).
- 2) Write down the <u>question numbers</u>, <u>your answers</u>, and <u>your student ID</u> on **BLANK A4 PAPERS**.
 - Questions? Please "Raise Hand" in Zoom, and then you will be moved to a breakroom for asking questions.
- 3) During the whole answering phase:
 - Please STAY CONNECTED and START VIDEO in Zoom;
 - Please PREPARE all the materials BEFOREHAND;
 - Please do NOT use your cell phone;
 - Please do NOT use any instant messaging software nor communicate with anyone else in any means.

Honesty is the Best Policy!

③ Submission (after 11:30am)



- 1) Take **clear photos** of what you have written on A4 papers (write down your SID on every pages).
- 2) Submit all the photos to **Blackboard**.
 - The submission link will be available <u>after 11:30am</u>.
 - Early-submission will be NOT accepted.
 - All image formats or PDF format are accepted.

ASSIGNMENT SUBMISSION					
Text Submission Write Submission					
Attach Files Browse Local Files	Browse Course Files	Browse Cloud Service			

3) WAIT until tutors have confirmed your submission.

Fake Exam



- To get you familiar with the procedure of the online exam, a **fake exam** will be held on April 20, 2021.
 - The fake exam will be available from 4:30 PM to 6:15 PM (i.e., lab sessions) on April 20, 2021.
 - The fake exam papers and submission link will be both located at "Course Contents" → "Exam" in Blackboard.

	 2020R2 Rapid Prototyping of Digital Systems (CENG3430) 	Course Contents				
	Notifications Announcements	Exam S				
D	Course Outline Course Contents	Lecture Notes Build Content v Assessments v Tools v Partner Content v				
	Discussion Board Groups My Grades	Lecture Recordings ► Availability: Item is hidden from students. It will be available after Apr 20, 2021 4:30 PM. Enabled: Statistics Tracking				
	Library Reading List	Lab Exercises Fake Exam Submission Availability: Item is hidden from students. It will be available after Apr 20, 2021 4:30 PM.				
	Panopto Video	Lab Recordings				

Preparation Tips for Final Exam



- The scope covers Lec01~Lec10 and Lab01~Lab10.
 - Review all the "lecture notes" and "lab sheets";
 - Review all the "Class Exercises" in Lec01~Lec10;
 - Review all the "required settings" and "provided/sample codes" for Lab01~Lab10 as well.
- We use several types of programming languages:
 VHDL, Verilog, C, and Shell scripts.
 - Make sure you can "interpret" codes programmed in any of these programming languages;
 - Make sure you can "write" (pseudo) codes in any of these programming languages (minor syntax mistakes are fine);
 - Make sure you can also "describe" hardware design in alternative ways (e.g., schematic circuit and FSM).